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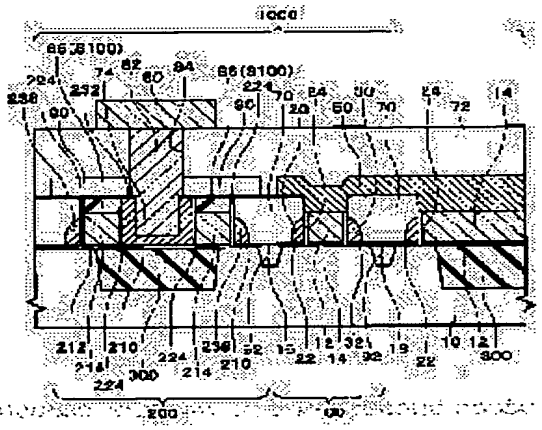
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device comprising an MONOS type nonvolatile memory, and to provide its manufacturing method.
SOLUTION: The semiconductor device comprises a memory cell 100. The memory cell 100 comprises a word gate 14 formed on a semiconductor substrate 10 through a second gate insulation layer 12, impurity layers 16 and 18, and first and second sidewall-like control gates 20 and 30. A set of first and second control gates abutting on each other through the impurity layers 16 and 18 are connected with a common contact part 200. The common contact part 200 comprises a contact conductive layer 232, a stopper layer 86, and a cap insulation layer 90. The contact conductive layer 232 is connected with the first and second control gates 20 and 30. The cap insulation layer 90 is formed at least on a stopper insulation layer 86.



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CLAIMS

[Claim(s)]

[Claim 1] It has the memory cell array by which the nonvolatile storage was arranged by two or more lines and trains in the shape of a grid. Said nonvolatile storage The WORD gate formed above the semi-conductor layer through the 2nd gate insulating layer, The impurity layer which constitutes the source field or drain field formed in said semi-conductor layer, The 1st and 2nd control gate of the shape of a sidewall formed along one side face of said WORD gate, and the side face of another side, respectively, An implication and said 1st control gate mind the 1st gate insulating layer to said semi-conductor layer. It is arranged through the 1st side insulating layer to said WORD gate. And said 2nd control gate It is arranged through the 1st side insulating layer through the 1st gate insulating layer to said WORD gate to said semi-conductor layer. Said 1st and 2nd control gate 1 set of 1st and 2nd control gates which adjoin each other through said impurity layer to the 2nd direction which is arranged succeeding the 1st direction, respectively and intersects said 1st direction It connects with the common contact section. Said common contact section A contact conductive layer, a stopper insulating layer, and a cap insulating layer are included. Said contact conductive layer It is the semiconductor device with which said stopper insulating layer is continuously arranged with said 1st and 2nd control gate on the outside of said contact conductive layer, and said cap insulating layer is formed above said stopper insulating layer at least.

[Claim 2] It is the semiconductor device with which said contact conductive layer is arranged through the 2nd side insulating layer inside said cap insulating layer in claim 1.

[Claim 3] It is the semiconductor device which consists of the quality of the material as said 1st and 2nd control gate with said same contact conductive layer in claims 1 or 2.

[Claim 4] The semiconductor device with which the top face of said contact conductive layer and the top face of said stopper insulating layer constitute a flat surface mostly in claim 1 thru/or either of 3.

[Claim 5] It is the semiconductor device

which consists of an ingredient with which said cap insulating layer uses silicon oxide as a principal component by said stopper insulating layer consisting of an ingredient which uses silicon nitride as a principal component in claim 1 thru/or either of 4.

[Claim 6] It is the semiconductor device with which said contact conductive layer constitutes a crevice, the contact hole which penetrates said cap insulating layer and said layer insulation layer is formed on this crevice, and the plug conductive layer is embedded in said contact hole by carrying out the laminating of the layer insulation layer above said cap insulating layer further in claim 1 thru/or either of 5.

[Claim 7] It is the semiconductor device which said contact conductive layer is arranged through a contact insulating layer above said semi-conductor layer in claim 2 thru/or either of 6, and consists of the quality of the material as said 1st gate insulating layer with said same contact insulating layer.

[Claim 8] It is the semiconductor device which consists of the quality of the material as said 1st side insulating layer with said same 2nd side insulating layer in claim 3 thru/or either of 7.

[Claim 9] Said 1st side insulating layer located between said WORD gates and said control gates in claim 1 thru/or either of 8 is a semiconductor device with which the upper limit is located to said semi-conductor layer more nearly up than said control gate.

[Claim 10] Said 1st and 2nd control gate which adjoins each other in claim 1 thru/or either of 9 is a semiconductor device currently embedded by the insulating layer.

[Claim 11] It is the semiconductor device which said common contact section adjoined the edge of said impurity layer in claim 1 thru/or either of 10, and was formed.

[Claim 12] It is the semiconductor device formed by turns in one near edge of this impurity layer, and the near edge of another side to said impurity layer by which two or more arrays of said common contact section were carried out in claim 11.

[Claim 13] It is the semiconductor device with which said 1st gate insulating layer and said 1st side insulating layer consist of a cascade screen of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer in claim 1 thru/or either of 12.

[Claim 14] The manufacture approach of a semiconductor device which a nonvolatile storage is the manufacture approach of the semiconductor device which contains in two or more lines and trains the memory cell array arranged in the shape of a grid, and includes the following processes.

The process which forms the 1st insulating layer for the 2nd gate

insulating layer above a semi-conductor layer, Patterning of the process which forms a stopper layer above the process which forms the 1st conductive layer above said 1st insulating layer, and said 1st conductive layer, said 1st conductive layer, and said stopper layer is carried out. The process which forms a gate layer, the process which forms the 1st gate insulating layer above said semi-conductor layer at least, A mask is formed on said 2nd conductive layer corresponding to the formation field of the process which forms the 1st side insulating layer in the both-sides side of said gate layer, the process which forms the 2nd conductive layer in the formation field of said memory cell array, and the common contact section. The process which forms the sidewall-like 1st and 2nd control gate by carrying out anisotropic etching of said 2nd conductive layer, By grinding this 2nd insulating layer and said 2nd conductive layer by the chemical mechanical grinding method so that said stopper layer may be exposed after forming the 2nd insulating layer in the formation field of said memory cell array The process which forms a contact conductive layer in the formation field of said common contact section, The process which forms in said semi-conductor layer the impurity layer which constitutes a source field or a drain field, By forming a mask on said 3rd insulating layer corresponding to the formation field of the common contact section, and carrying out patterning of said 3rd insulating layer, after forming the 3rd insulating layer for a cap insulating layer in the formation field of said memory cell array After forming the 3rd conductive layer in the process which forms said cap insulating layer in the formation field of said common contact section, and the formation field of said memory cell array, patterning of said gate layer, said 3rd conductive layer, and said stopper layer is carried out. The process which forms a stopper insulating layer in the formation field of said common contact while forming the word line connected to said WORD gate and this WORD gate.

[Claim 15] The process which carries out patterning of said gate layer in claim 14 is the manufacture approach including the process which forms said stopper insulating layer above said 1st conductive layer of a semiconductor device.

[Claim 16] The manufacture approach including the process which forms further the contact hole which penetrates said cap insulating layer and said layer insulation layer on said contact conductive layer in claims 14 or 15 after forming a layer insulation layer in the formation field of said memory cell array, and the process which embeds a plug conductive layer in said contact hole of a semiconductor device.

[Claim 17] The manufacture approach of a semiconductor device which forms said

stopper layer in claim 14 thru/or either of 16 from the ingredient which uses silicon nitride as a principal component, and forms said 3rd insulating layer from the ingredient which uses silicon oxide as a principal component.

[Claim 18] It is the manufacture approach of a semiconductor device which said 1st gate insulating layer and said 1st side insulating layer are formed at the same membrane formation process in claim 15 thru/or either of 17, and consists of a cascade screen of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer.

[Claim 19] It is the manufacture approach of a semiconductor device formed in claim 15 thru/or either of 18 at the membrane formation process as said control gate that said contact conductive layer is the same.

[Claim 20] In claim 15 thru/or either of 19, it sets to the formation field of said common contact section. The process which forms a contact insulating layer above said semi-conductor layer, and the process which forms the 2nd side insulating layer in the side face of said contact conductive layer are included. Furthermore, formation of said contact insulating layer It is the manufacture approach of a semiconductor device which is performed at the same process as the process which forms said 1st gate insulating layer, and is performed at the process as the process which forms said 1st side insulating layer that formation of said 2nd side insulating layer is the same.

[Claim 21] The manufacture approach of a semiconductor device which forms said 1st side insulating layer in claim 15 thru/or either of 21 so that the upper limit may be located to said semi-conductor layer more nearly up than said control gate.

[Claim 22] Said 1 set which adjoins each other through said impurity layer in the process which grinds said 2nd insulating layer by the chemical mechanical grinding method in claim 15 thru/or either of 22 of control gates are the manufacture approaches of a semiconductor device formed so that it may be covered with a pad insulating layer.

[Claim 23] It is the manufacture approach of a semiconductor device which said common contact section adjoins the edge of said impurity layer in claim 15 thru/or either of 23, and is formed.

[Claim 24] It is the manufacture approach of a semiconductor device formed by turns in one near edge of this impurity layer, and the near edge of another side to said impurity layer by which two or more arrays of said common contact section were carried out in claim 15 thru/or either of 24.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device with which the nonvolatile storage which has two charge storage fields to the one WORD gate has been arranged in the shape of an array, and its manufacture approach.

[0002]

[A background technique and Object of the Invention] As one type of a non-volatile semiconductor memory, the gate insulating layer between a channel field and the control gate consists of a cascade screen of a silicon oxide layer and a silicon nitride layer, and there is a type called the MONOS (Metal Oxide Nitride Oxide Semiconductor) mold or SONOS (Silicon Oxide Nitride Oxide Silicon) mold with which the trap of the charge is carried out to said silicon nitride layer.

[0003] The device shown in drawing 15 is known as a non-volatile semiconductor memory of a MONOS mold (reference: Y.Hayashi, et al , 2000 Symposium - VLSI TechnologyDigest of Technical Papers p.122-p.123).

[0004] As for this MONOS type of memory cell 100, the WORD gate 14 is formed above the semi-conductor substrate 10 through the 2nd gate insulating layer 12. And in both the sides of the WORD gate 14, sidewall-like the 1st control gate 20 and the 2nd control gate 30 are arranged, respectively. The 1st gate insulating layer 22 exists between the pars basilaris ossis occipitalis of the 1st control gate 20, and the semi-conductor substrate 10, and an insulating layer 24 exists between the side face of the 1st control gate 20, and the WORD gate 14. Similarly, the 1st gate insulating layer 32 exists between the pars basilaris ossis occipitalis of the 2nd control gate 30, and the semi-conductor substrate 10, and an insulating layer 34 exists between the side face of the 2nd control gate 30, and the WORD gate 14. And the impurity layers 16 and 18 which constitute a source field or a drain field are formed in the semi-conductor substrate 10 between the control gates 20 and the control gates 30 of an adjacent memory cell which counter.

[0005] Thus, one memory cell 100 has two MONOS mold memory devices on the side face of the WORD gate 14. Moreover, these two MONOS mold memory devices are controlled independently. Therefore, one memory cell 100 can memorize 2-bit information.

[0006] The purpose of this invention is to offer the semiconductor device containing the nonvolatile storage of the MONOS mold which has two charge storage fields, and its manufacture approach.

[0007]

[Means for Solving the Problem] (Semiconductor device) The semiconductor device concerning this invention It has the memory cell array by which the nonvolatile storage was arranged by two or more lines and trains in the shape of a grid. Said nonvolatile storage The WORD gate formed above the semi-conductor layer through the 2nd gate insulating layer, The impurity layer which constitutes the source field or drain field formed in said semi-conductor layer, The 1st and 2nd control gate of the shape of a sidewall formed along one side face of said WORD gate, and the side face of another side, respectively, An implication and said 1st control gate mind the 1st gate insulating layer to said semi-conductor layer. It is arranged through the 1st side insulating layer to said WORD gate. And said 2nd control gate It is arranged through the 1st side insulating layer through the 1st gate insulating layer to said WORD gate to said semi-conductor layer. Said 1st and 2nd control gate 1 set of 1st and 2nd control gates which adjoin each other through said impurity layer to the 2nd direction which is arranged succeeding the 1st direction, respectively and intersects said 1st direction It connects with the common contact section. Said common contact section A contact conductive layer, a stopper insulating layer, and a cap insulating layer are included. Said contact conductive layer Said stopper insulating layer is continuously arranged with said 1st and 2nd control gate on the outside of said contact conductive layer, and said cap insulating layer is formed above said stopper insulating layer at least.

[0008] According to the semiconductor device concerning this invention, since it connects with the common contact section for every set, the sidewall-like control gate can take certainly electrical installation with the small control gate of width of face.

[0009] The semiconductor device of this invention can take the following various modes.

[0010] (A) Said contact conductive layer can be arranged through the 2nd side insulating layer inside said cap insulating layer. In addition, said 2nd side insulating layer can be formed in this case from the same quality of the material as said 1st side insulating layer.

[0011] Moreover, said contact conductive layer can consist of the same quality of the material as said 1st and 2nd control gate in this case.

[0012] (B) The top face of said contact conductive layer and the top face of said stopper insulating layer can constitute a flat surface mostly.

[0013] (C) Said stopper insulating layer consists of an ingredient which uses silicon nitride as a principal component, and said cap insulating layer can consist of an ingredient which uses silicon oxide

as a principal component.

[0014] (D) The laminating of the layer insulation layer is further carried out above said cap insulating layer, a crevice is constituted, the contact hole which penetrates said cap insulating layer and said layer insulation layer is formed on this crevice, and said contact conductive layer can embed a plug conductive layer in said contact hole.

[0015] (E) Said contact conductive layer is arranged through a contact insulating layer above said semi-conductor layer, and said contact insulating layer can consist of the same quality of the material as said 1st gate insulating layer.

[0016] (F) The upper limit of said 1st side insulating layer located between said WORD gates and said control gates can be located to said semi-conductor layer more nearly up than said control gate. By this configuration, a wrap pad insulating layer can be certainly formed for said control gate. That is, said adjacent 1st and 2nd control gate is covered with a pad insulating layer, and this pad insulating layer is formed between said two side insulating layers which has been arranged in contact with said 1st and 2nd control gate and which counters.

[0017] (G) Said adjacent 1st and 2nd control gate can be embedded by the insulating layer.

[0018] (H) Said common contact section can be adjoined and prepared in the edge of said impurity layer. And said common contact section can be prepared by turns to said impurity layer by which two or more arrays were carried out in one near edge of this impurity layer, and the near edge of another side.

[0019] (I) Said 1st gate insulating layer and the 1st side insulating layer can consist of cascade screens of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer.

[0020] (The manufacture approach of a semiconductor device) A nonvolatile storage is the manufacture approach of the semiconductor device which contains in two or more lines and trains the memory cell array arranged in the shape of a grid, and the manufacture approach concerning this invention includes the following processes.

[0021] The process which forms the 1st insulating layer for the 2nd gate insulating layer above a semi-conductor layer, Patterning of the process which forms a stopper layer above the process which forms the 1st conductive layer above said 1st insulating layer, and said 1st conductive layer, said 1st conductive layer, and said stopper layer is carried out. The process which forms a gate layer, the process which forms the 1st gate insulating layer above said semi-conductor layer at least, A mask is formed on said 2nd conductive layer corresponding to the formation field of the process which forms the 1st side insulating layer in the both-sides side of

said gate layer, the process which forms the 2nd conductive layer in the formation field of said memory cell array, and the common contact section. The process which forms the sidewall-like 1st and 2nd control gate by carrying out anisotropic etching of said 2nd conductive layer, By grinding this 2nd insulating layer and said 2nd conductive layer by the chemical mechanical grinding method so that said stopper layer may be exposed after forming the 2nd insulating layer in the formation field of said memory cell array The process which forms a contact conductive layer in the formation field of said common contact section, The process which forms in said semi-conductor layer the impurity layer which constitutes a source field or a drain field, By forming a mask on said 3rd insulating layer corresponding to the formation field of the common contact section, and carrying out patterning of said 3rd insulating layer, after forming the 3rd insulating layer for a cap insulating layer in the formation field of said memory cell array After forming the 3rd conductive layer in the process which forms said cap insulating layer in the formation field of said common contact section, and the formation field of said memory cell array, patterning of said gate layer, said 3rd conductive layer, and said stopper layer is carried out. The process which forms a stopper insulating layer in the formation field of said common contact while forming the word line connected to said WORD gate and this WORD gate.

[0022] According to the manufacture approach of the semiconductor device concerning this invention, with the sidewall-like 1st and 2nd control gate, the common contact section can be formed and positive electrical installation can be taken through this common contact section.

[0023] The mode illustrated further below can be taken in the manufacture approach concerning this invention.

[0024] (a) The process which carries out patterning of said gate layer can include the process which forms said stopper insulating layer above said 1st conductive layer.

[0025] In this case, said contact conductive layer can be formed at the same membrane formation process as said control gate.

[0026] Moreover, the process which forms a contact insulating layer above said semi-conductor layer further in the formation field of said common contact section in this case, The process which forms the 2nd side insulating layer in the side face of said contact conductive layer is included. Formation of said contact insulating layer It is carried out at the same process as the process which forms said 1st gate insulating layer, and formation of said 2nd side insulating layer is performed at the same process as the process which forms said 1st side

insulating layer.

[0027] (b) Further, after forming a layer insulation layer in the formation field of said memory cell array, the process which forms the contact hole which penetrates said cap insulating layer and said layer insulation layer on said contact conductive layer, and the process which embeds a plug conductive layer in said contact hole can be included.

[0028] (c) Said stopper layer can be formed from the ingredient which uses silicon nitride as a principal component, and said 3rd insulating layer can be formed from the ingredient which uses silicon oxide as a principal component.

[0029] (d) Said 1st gate insulating layer and said 1st side insulating layer are formed at the same membrane formation process, and can consist of a cascade screen of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer.

[0030] (e) The upper limit of said 1st side insulating layer can be formed so that it may be located to said semi-conductor layer more nearly up than said control gate.

[0031] (f) In the process which grinds said 2nd insulating layer by the chemical mechanical grinding method (henceforth the "CMP method"), said 1 set which adjoins each other through said impurity layer of control gates can be formed so that it may be covered with a pad insulating layer.

[0032] (g) Said common contact section can be adjoined and formed in the edge of said impurity layer. Moreover, said common contact section can be formed by turns to said impurity layer by which two or more arrays were carried out in one near edge of this impurity layer, and the near edge of another side.

[0033]

[Embodiment of the Invention] Drawing 1 is the top view showing typically the layout of the memory cell array which constitutes the semiconductor device concerning the gestalt of operation of this invention, drawing 2 is the top view showing typically some semiconductor devices concerning the gestalt of this operation, and drawing 3 is the sectional view showing typically the part which met the A-A line of drawing 2 .

[0034] The semiconductor device concerning the gestalt of this operation contains the memory cell array 1000 by which the MONOS mold nonvolatile storage (henceforth a "memory cell") 100 was arranged by two or more lines and trains in the shape of a grid. Moreover, this memory cell array 1000 is divided into two or more blocks.

[0035] (Structure of a device) The layout of the semiconductor device concerning the gestalt of this operation is explained first, referring to drawing 1 .

[0036] In drawing 1 , the 1st block B1 and 2nd block B-2 which adjoins this are shown. the part between the 1st block B1

and 2nd block B-2 -- the component isolation region 300 is formed in the field. In each block B1 and B-2, two or more word lines 50 (WL) prolonged in the direction of X (line writing direction) and two or more bit lines 60 (BL) prolonged in the direction (the direction of a train) of Y are formed. One word line 50 is connected to two or more WORD gates 14 arranged in the direction of X. The bit line 60 is constituted by the impurity layers 16 and 18.

[0037] The conductive layer 40 which constitutes the 1st and 2nd control gates 20 and 30 is formed so that each impurity layers 16 and 18 may be surrounded. That is, the 1st and 2nd control gates 20 and 30 have extended in the direction of Y, respectively, and one edge of 1 set of 1st and 2nd control gates 20 and 30 is mutually connected by the conductive layer prolonged in the direction of X. Moreover, both the other end sections of 1 set of 1st and 2nd control gates 20 and 30 are connected to the one common contact section 200. therefore, every -- the 1st and 2nd control gates 20 and 30 have the function of the control gate of a memory cell, and a function as wiring which connects each control gate arranged in the direction of Y.

[0038] Moreover, this common contact section 200 is adjoined and formed in the edge of the impurity layers 16 and 18, as shown in drawing 1 R> 1. Furthermore, this common contact section 200 is formed by turns to the impurity layers 16 and 18 in one near edge of the impurity layers 16 and 18, and the near edge of another side.

[0039] The single memory cell 100 is the outside of the one WORD gate 14, the 1st and 2nd control gates 20 and 30 formed in the both sides of this WORD gate 14, and these control gates 20 and 30, and contains the impurity layers 16 and 18 formed in the semi-conductor substrate. And the impurity layers 16 and 18 are shared by the memory cell 100 which adjoins each other, respectively.,

[0040] It is the impurity diffused layer 16 which adjoins each other in the direction of Y mutually, and the impurity layer 16 formed in the block B1 and the impurity layer 16 of each other formed in block B-2 are electrically connected by the impurity layer 400 for contact formed in the semi-conductor substrate. This impurity layer 400 for contact is formed in the opposite side in the common contact section 200 of the control gate to an impurity 16.

[0041] Contact 350 is formed on this impurity layer 400 for contact. The bit line 60 constituted by the impurity layer 16 is electrically connected to the upper wiring layer by this contact 350.

[0042] Similarly, two impurity layers 18 of each other which adjoin each other in the direction of Y mutually are electrically connected by the impurity layer for contact which is not illustrated

to the side by which the common contact section 200 is not arranged.

[0043] In one block, the flat-surface layout of two or more common contact sections 200 serves as alternate arrangement so that drawing 1 may show. Similarly, in one block, the flat-surface layout of two or more impurity layers 400 for contact serves as alternate arrangement.

[0044] Next, the planar structure and cross-section structure of a semiconductor device are explained, referring to drawing 2 and drawing 3 .

[0045] A memory cell 100 includes the WORD gate 14 formed above the semi-conductor substrate 10 through the 2nd gate insulating layer 12, the impurity layers 16 and 18 which constitute the source field or drain field formed in the semi-conductor substrate 10, and the sidewall-like 1st and the 2nd control gate 20 and 30 which were formed along with the both sides of the WORD gate 14, respectively. Moreover, the silicide layer 92 is formed on the impurity layer 16 and 18.

[0046] The 1st control gate 20 is arranged through the 2nd gate insulating layer 12 above the semi-conductor substrate 10, and is arranged through the 1st side insulating layer 24 to one side face of the WORD gate 14. Similarly, the 2nd control gate 30 is arranged through the 2nd gate insulating layer 32 to the semi-conductor substrate 10, and is arranged through the 1st side insulating layer 34 to the side face of another side of the WORD gate 14.

[0047] And the 1st gate insulating layers 22 and 32 and the 1st side insulating layers 24 and 34 are ONO film. Specifically, it is the cascade screen of the 1st silicon oxide layer (bottom silicon oxide layer), a silicon nitride layer, and the 2nd silicon oxide layer (top silicon oxide layer).

[0048] The 1st silicon oxide layer of the 1st gate insulating layers 22 and 32 functions as a potential barrier (potential barrier) between a channel field and a charge storage field.

[0049] The silicon nitride layer of the 1st gate insulating layers 22 and 32 functions as a charge storage field which carries out the trap of the carrier (for example, electron).

[0050] The 2nd silicon oxide layer of the 1st gate insulating layers 22 and 32 forms a potential barrier (potential barrier) between the control gate and a charge storage field.

[0051] The 1st side insulating layers 24 and 34 make the WORD gate 14 and the 1st and 2nd control gates 20 and 30 separate electrically, respectively. Moreover, the upper limit of the 1st side insulating layers 24 and 34 is located up to the semi-conductor substrate 10 compared with the upper limit of the 1st and 2nd control gates 20 and 30, in order to prevent short-circuit with the WORD gate 14 and the 1st and 2nd control gates

20 and 30.

[0052] With the gestalt of this operation, it is formed at the membrane formation process that the 1st side insulating layers 24 and 34 and the 1st gate insulating layers 22 and 32 are the same, and each layer structure becomes equal. Furthermore, the 1st side insulating layers 24 and 34 are formed so that the upper limit may be located to the semi-conductor substrate 10 more nearly up than the 1st and 2nd control gates 20 and 30. And in the adjacent memory cell 100, the embedding insulating layer 70 is formed between adjacent 1st control gates 20 and 2nd control gates 30. In the gestalt of this operation, the 1st and 2nd control gates 20 and 30 are embedded by the embedding insulating layer 70. This embedding insulating layer 70 has covered these so that the 1st and 2nd control gates 20 and 30 may not be exposed at least. Specifically, the top face of the embedding insulating layer 70 is located from the upper limit of the 1st side insulating layers 24 and 34 up to the semi-conductor substrate 10. By forming the embedding insulating layer 70 in this way, electrical isolation of the 1st and 2nd control gates 20 and 30, and the WORD gate 14 and a word line 50 can be performed more certainly.

[0053] The conductive layer for supplying predetermined potential to the 1st and 2nd control gates 20 and 30 is formed in the common contact section 200. The common contact section 200 mainly contains the contact conductive layer 232, the stopper insulating layer 86, and the cap insulating layer 90.

[0054] The contact conductive layer 232 is arranged through the 2nd side insulating layer 224 inside the stopper insulating layer 86 and the conductive layer 214. Of the same membrane formation process as formation of the 1st and 2nd control gates 20 and 30, the contact conductive layer 232 is formed so that the 1st and 2nd control gates 20 and 30 may be followed. Therefore, it is formed with the quality of the material with same contact conductive layer 232 and 1st and 2nd control gates 20 and 30.

[0055] Moreover, this contact conductive layer 232 is arranged through the contact insulating layer 210 above the semi-conductor substrate 10. Furthermore, a crevice 74 is constituted by this contact conductive layer 232, and the plug conductive layer 82 mentioned later is embedded in this crevice 74.

[0056] Moreover, the layer insulation layer 72 is formed on the cap insulating layer 90, the word line 50, and the embedding insulating layer 70 in which these are not formed. And on the crevice 74 formed of the contact conductive layer 232, the contact hole 84 which penetrates the cap insulating layer 90 and the layer insulation layer 72 is formed. That is, this contact hole 84 penetrated the cap insulating layer 90 and the layer

insulation layer 72, and has reached to the contact conductive layer 232. In this contact hole 84, the plug conductive layer 82 which consists of a tungsten plug or a copper plug is embedded.

[0057] The stopper insulating layer 86 is arranged on the outside of the contact conductive layer 232, as shown in drawing 3 . Moreover, the stopper insulating layer 86 is formed on the conductive layer 214 mentioned later. The stopper insulating layer 86 consists of an ingredient which uses silicon nitride as a principal component. In the gestalt of this operation, the top face of the contact conductive layer 232 and the top face of the stopper insulating layer 86 can form so that a flat surface may be constituted mostly.

[0058] The cap insulating layer 90 is formed on the stopper insulating layer 86 at least. The cap insulating layer 90 consists of an ingredient which uses silicon oxide as a principal component.

[0059] Moreover, the common contact section 200 contains a conductive layer 214 and a conductive layer 236,238 further.

[0060] A conductive layer 214 is formed at the same membrane formation process as the WORD gate 14. In this case, a conductive layer 214 is formed from the same quality of the material as the WORD gate 14. In the gestalt of this operation, the conductive layer 214 is arranged through the insulating layer 212 above the semi-conductor substrate 10.

[0061] The insulating layer 212 which constitutes the common contact section 200 is formed at the same process as the 2nd gate insulating layer 12 which constitutes a memory cell 100, and has the same layer structure. Moreover, it is formed at the same process as the contact insulating layer 210, the 1st gate insulating layers 22 and 32 from which the 2nd side insulating layer 224 constitutes a memory cell 100 by reaching, and the 1st side insulating layers 24 and 34 which constitute the common contact section 200, and has the same layer structure. That is, it reaches contact insulating layer 210, and the 2nd side insulating layer 224 consists of cascade screens of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer like the 1st gate insulating layers 22 and 32 and the 1st side insulating layers 24 and 34.

[0062] Moreover, as shown in drawing 3 , the common contact section 200 contains the sidewall-like conductive layer 236,238 further. This conductive layer 236 is following the 1st control gate 20. Here, the 1st control gate 20 which follows a conductive layer 236 adjoins the 2nd control gate 30 which follows the contact conductive layer 232. Moreover, the conductive layer 238 is following the 2nd control gate 30. Here, the 2nd control gate 30 which follows a conductive layer

238 adjoins the 1st control gate 20 which follows the contact conductive layer 232.

[0063] A conductive layer 236,238 is arranged through the 2nd side insulating layer 224 on one side face of a conductive layer 214, respectively. This conductive layer 236,238 is formed from the same membrane formation process as the 1st and 2nd control gates 20 and 30 or the contact conductive layer 232, and consists of the same quality of the material as these layers.

[0064] In addition, in the semiconductor device of the gestalt of this operation, although the case where a conductive layer 236,238 was a sidewall-like was shown, the configuration of a conductive layer 236,238 is not necessarily limited to this.

[0065] According to the semiconductor device concerning the gestalt of this operation, in the memory cell array 1000, the sidewall-like 1st and 2nd control gates 20 and 30 are connected with the common contact section 200 for every set. This common contact section 200 can take electrical installation with these control gates certainly including the contact conductive layer 232, the stopper insulating layer 86 formed in the outside of this contact conductive layer, and the cap insulating layer 90 by forming the cap insulating layer 90 on the stopper insulating layer 86 at least. That is, the control gates 20 and 30 of the semiconductor device of the gestalt of this operation have a sidewall-like configuration, and the width of face is usually smaller than 0.1 micrometers. Therefore, the electrical installation of the control gates 20 and 30 and the common contact section 200 is securable with the contact conductive layer 232. Consequently, electric contact to the control gate is securable in a necessary minimum area with the above-mentioned common contact section.

[0066] (The manufacture approach of a semiconductor device) Next, the manufacture approach of the semiconductor device concerning the gestalt of this operation is explained, referring to drawing 4 - Fig. 1414 . Each sectional view corresponds to the part which met the A-A line of drawing 2 . In drawing 4 - drawing 14 , the same sign is substantially given to the same part with the part shown by drawing 1 R> 1 - drawing 3, and the overlapping publication is omitted.

[0067] (1) field (henceforth "formation field of memory cell array") 1000a in which the memory cell array 1000 shown in drawing 1 is first formed as shown in drawing 4 -- setting -- the front face of the semi-conductor substrate 10 -- LOCOS -- form the component isolation region 300 by law or the trench isolation method. Subsequently, the impurity layer 400 (refer to drawing 1) for contact is formed in the semi-conductor substrate 10 by the ion implantation.

[0068] Subsequently, the 1st gate insulating layer and the 1st becoming insulating layer 120 are formed in the front face of the semi-conductor substrate 10. Subsequently, the WORD gate 14, a conductive layer 214, and the 1st becoming conductive layer 140 are deposited on the 1st insulating layer 120. The 1st conductive layer 140 consists of a doped polysilicon. Subsequently, the stopper layer S100 in a next CMP process is formed on the 1st conductive layer 140. The stopper layer S100 consists for example, of a silicon nitride layer.

[0069] (2) Subsequently, carry out patterning of the 1st conductive layer 140 and the stopper layer S100 by well-known lithography and well-known etching. Of this process, the WORD gate and becoming gate layer 140a are formed in behind. In this patterning, the layered product of gate layer 140a and the stopper layer S100 is extensively formed on the semi-conductor substrate 10 in formation field 1000a of a memory cell array. Drawing 6 showed the situation after patterning superficially. As for the layered product of gate layer 140a in a memory area 1000, and the stopper layer S100, opening 160,180 is formed by this patterning. Opening 160,180 supports mostly the field in which the impurity layers 16 and 18 are formed of a next ion implantation. And the 1st side insulating layers 24 and 34 and the 1st and 2nd control gates 20 and 30 are formed along the side face of opening 160,180 at a next process.

[0070] (3) As shown in drawing 7 , form the ONO film 220 extensively on the semi-conductor substrate 10. The ONO film 220 is formed by carrying out the sequential deposition of the 1st silicon oxide layer, a silicon nitride layer, and the 2nd silicon oxide layer. The 1st silicon oxide layer can be formed using for example, the oxidizing [thermally] method and a CVD method. A silicon nitride layer can be formed with a CVD method etc. The 2nd silicon oxide layer can be formed using voloxidation (HTO) on a CVD method and a concrete target. After forming these each class, it is desirable to perform annealing treatment and to carry out eburnation of each class.

[0071] The ONO film 220 serves as the 1st gate insulating layer 22, the 1st side insulating layer 24, the contact insulating layer 210 of the common contact section 200, and the 2nd side insulating layer 224 by next patterning (refer to drawing 3).

[0072] (4) As shown in drawing 8 , form extensively the doped polysilicon layer (the 2nd conductive layer) 230 on the ONO film 220 in formation field 1000a of a memory cell array. From this doped polysilicon layer 230, the conductive layer 40 (refer to drawing 1) which constitutes the 1st and 2nd control gates 20 and 30 through patterning, an etching process, etc. and the contact conductive layer 232

which constitutes the common contact section 200, and a conductive layer 236,238 (refer to drawing 3) are formed.

[0073] Subsequently, the resist layer R100 is formed in field (henceforth "formation field of the common contact section") 200a in which the common contact section is formed. With the gestalt of this operation, this resist layer R100 is mostly formed in the location corresponding to formation field 200a of the common contact section, as shown in drawing 8 . This resist layer R100 is formed on the field in which the contact conductive layer 232 formed at a next process is formed at least.

[0074] (5) As shown in drawing 9 , the 1st and 2nd control gates 20 and 30, contact conductive layer 230a, and a conductive layer 236,238 are formed in the doped polysilicon layer 230 (refer to drawing 8) by carrying out anisotropic etching of the resist layer R100 extensively as a mask. Here, contact conductive layer 230a and a conductive layer 236,238 are formed in formation field 200a of the common contact section.

[0075] That is, the sidewall-like 1st and 2nd control gates 20 and 30 and a conductive layer 236,238 are formed along the side face of the exposed opening 160,180 (refer to drawing 6) of this etching process. And contact conductive layer 230a is formed in the part by which could come, simultaneously the mask was carried out in the resist layer R100. Here, this contact conductive layer 230a is formed so that the 1st and 2nd control gates 20 and 30 may be followed. Furthermore, by the above-mentioned etching, the insulating layer deposited on the field in which a silicide layer is formed at a next process is removed, and the semi-conductor substrate 10 exposes it. Subsequently, the resist layer R100 is removed.

[0076] (6) Subsequently, as shown in drawing 10 , form the impurity layers 16 and 18 which constitute a source field or a drain field in the semi-conductor substrate 10 by carrying out the ion implantation of the N type impurity.

[0077] Subsequently, the metal for silicide formation is made to deposit extensively. The metals for silicide formation are titanium and cobalt. Then, the silicide layer 92 is made to form in the top face of the impurity layers 16 and 18 by making the impurity layer 16 and the metal formed on 18 silicide-ization react. Therefore, a memory cell 100 is silicide-ized by the silicide chemically-modified [this] degree in [the front face of a source field or a drain field] self align.

[0078] Subsequently, in formation field 1000a of a memory cell array, the insulating layers (the 2nd insulating layer) 70, such as silicon oxide or nitriding silicon oxide, are formed extensively. An insulating layer 70 is formed so that the stopper layer S100

may be covered and between the 1st and 2nd control gates 20 and 30 and the clearance between contact conductive layer 230a may be embedded.

[0079] (7) As shown in drawing 11 , using the CMP method, grind until the stopper layer S100 exposes an insulating layer 70, and carry out flattening of the insulating layer 70. By this polish, an insulating layer 70 remains between the two 1st side insulating layers 24 which counter across the 1st and 2nd control gates 20 and 30, and it becomes the pad insulating layer 70. Moreover, of this process, the upper part of contact conductive layer 230a is removed, and the contact conductive layer 232 is formed in formation field 200a of the common contact section.

[0080] At this time, the upper limit of the 1st side insulating layers 24 and 34 formed in the side face of gate layer 140a and the stopper layer S100 is located up to the semi-conductor substrate 10 compared with the upper limit of the 1st and 2nd control gates 20 and 30.

[0081] The 1st and 2nd control gates 20 and 30 are completely covered with this process by the embedding insulating layer 70. Moreover, in formation field 200a of the common contact section, it will be in the condition that the top face of the contact conductive layer 232 was exposed. Furthermore, the crevice 74 which consists of contact conductive layers 232 will be in the condition of having been embedded by the embedding insulating layer 70.

[0082] (8) Subsequently, as shown in drawing 12 , form 3rd insulating-layer 90a for forming the cap insulating layer 90 in the whole surface in formation field 1000a of a memory cell array. Then, the resist layer R200 by which patterning was carried out is formed on 3rd insulating-layer 90a. Patterning of the 3rd insulating-layer 90a is carried out by using this resist layer R200 as a mask, and as shown in drawing 13 , the cap insulating layer 90 is formed in formation field 200a of the common contact section. Subsequently, the resist layer R200 is removed.

[0083] Subsequently, the 3rd conductive layer (not shown) is formed in the whole surface in formation field 1000a of a memory cell array. After forming the 3rd conductive layer (not shown) in the whole surface, the resist layer R300 by which patterning was carried out is formed on the 3rd conductive layer. Patterning of said 3rd conductive layer is carried out by using this resist layer R300 as a mask, and a word line 50 is formed. As said 3rd conductive layer, alloy layers, such as a doped polysilicon layer, a metal layer, and silicide, or the layer which carried out the laminating more than of two-layer [of these] can be used. Furthermore, the conductive layer 214 by which the stopper insulating layer 86 was formed in the upper part with formation in the

WORD gate 14 arranged in the shape of an array is formed by carrying out patterning of the gate layer 140a (referring to drawing 12) which consists of a doped polysilicon by using the resist layer R300 as a mask. Subsequently, the resist layer R300 is removed.

[0084] In addition, at this etching process, since the 1st and 2nd control gates 20 and 30 and a conductive layer 236,238 are covered by the insulating layer 70, they remain, without being etched.

[0085] Subsequently, a P type impurity is extensively doped to the semi-conductor substrate 10. Thereby, the P type impurity layer (impurity layer for isolation) 15 (refer to drawing 2) is formed in the mutual field of the WORD gate 14 in the direction of Y. This impurity layer 15 for isolation consists of a conductivity type contrary to the conductivity type of a nonvolatile storage. Isolation between memory cell 100 is more certainly performed by this P type impurity layer 15.

[0086] (9) Subsequently, form the wiring layer electrically connected with this conductive layer after forming a contact hole by the well-known approach after carrying out the laminating of the layer insulation layer, and forming a conductive layer in a contact hole. For example, as shown in drawing 3 , after forming the contact hole 84 which penetrates the cap insulating layer 90 and the layer insulation layer 72 on the contact conductive layer 232 and embedding the plug conductive layer 82 in this contact hole 84, the wiring layer 80 connected with the plug conductive layer 82 is formed. In addition, in the process which forms a contact hole 84, after removing the insulating layer 70 currently embedded in the crevice 74 which consists of contact conductive layers 232, the plug conductive layer 82 is embedded in a crevice 74.

[0087] According to the above process, the semiconductor device shown in drawing 1 , drawing 2 , and drawing 3 can be manufactured.

[0088] According to the manufacture approach of the semiconductor device of the gestalt this operation, the common contact section 200 can be formed with the sidewall-like 1st and 2nd control gates 20 and 30, without making especially a routing counter increase. And the common contact section 200 can have the size near the width of face of the impurity layers 16 and 18 at least, and can secure a contact area big enough. Therefore, with the gestalt of this operation, even if it is the control gates 20 and 30 of the shape of a sidewall which cannot take sufficient KONTOKUTO field easily, positive electrical installation can be taken through the common contact section 200.

[0089] moreover, according to the manufacture approach of the semiconductor device of the gestalt this

operation, it is alike on the contact conductive layer 232, and the plug conductive layer 82 is formed. Here, the alignment allowances at the time of forming this plug conductive layer 82 are securable by installing the stopper insulating layer 86 in the outside of the contact conductive layer 232.

[0090] As mentioned above, although the gestalt of 1 operation of this invention was described, this invention is not limited to this but can take modes various by within the limits of the summary of invention of this invention. For example, with the gestalt of the above-mentioned implementation, although the bulk-like semi-conductor substrate was used as a semi-conductor layer, the semi-conductor layer of a SOI substrate may be used.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the top view showing typically the layout of the semiconductor device concerning the gestalt of operation of this invention.

[Drawing 2] It is the top view showing typically the important section of the semiconductor device concerning the gestalt of operation of this invention.

[Drawing 3] It is the sectional view showing typically the part which met the A-A line of drawing 2.

[Drawing 4] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 5] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 6] It is the top view showing one process of the manufacture approach of the semiconductor device shown in drawing 5.

[Drawing 7] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 8] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 9] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 10] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 11] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1.

[Drawing 12] It is the sectional view showing one process of the manufacture

approach of the semiconductor device shown in drawing 3 from drawing 1 .

[Drawing 13] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1 .

[Drawing 14] It is the sectional view showing one process of the manufacture approach of the semiconductor device shown in drawing 3 from drawing 1 .

[Drawing 15] It is the sectional view showing a well-known MONOS mold memory cell.

[Description of Notations]

10 Semi-conductor Substrate
12 2nd Gate Insulating Layer
14 WORD Gate
15 Impurity Layer for Isolation
16 18 Impurity layer
20 1st Control Gate
22 32 The 1st gate insulating layer
24 34 The 1st side insulating layer
30 2nd Control Gate
40 Conductive Layer
50 Word Line
60 Bit Line
70 Embedding Insulating Layer (2nd Insulating Layer)
72 Layer Insulation Layer
74 Crevice
80 Wiring Layer
82 Plug Conductive Layer
84 Contact Hole
86 Stopper Insulating Layer
90 Cap Insulating Layer
90a The 3rd insulating layer
92 Silicide Layer
100 Nonvolatile Storage (Memory Cell)
120 2nd Gate Insulating Layer (1st Insulating Layer)
122 Gate Insulating Layer
140 1st Conductive Layer
140a Gate layer
160,180 Opening
200 Common Contact Section
200a The formation field of the common contact section
210 Contact Insulating Layer
212 Insulating Layer
214 Conductive Layer
220 ONO Film (Dielectric Layer)
224 2nd Side Insulating Layer
230 Doped Polysilicon Layer (2nd Conductive Layer)
230a Contact conductive layer
232 Contact Conductive Layer
236 Conductive Layer
238 Conductive Layer
300 Component Isolation Region
350 Contact
400 Impurity Layer for Contact
S100 Stopper layer
R100, R200, R300 Resist layer
1000 Memory Cell Array
1000a The formation field of a memory cell array

[Translation done.]

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